REMARKS

I. Introduction

Applicants would like to thank Examiner Le for the indication of allowance of claims 6-8 and 13-15, and for the indication of allowable subject matter recited by claims 2 and 3. For the reasons set forth below, Applicants respectfully submit that remaining claim 1 is patentable over the cited prior art references.

II. The Rejection Of Claim 1 Under 35 U.S.C. § 102

Claim 1 is rejected under 35 U.S.C. § 102(b) as being anticipated by USP No. 5,198,706 to Papaliolios. Applicants respectfully traverse this rejection for at least the following reasons.

Claim 1 recites in-part a first ferroelectric capacitor which connects the second data input/output line to the first node, and a second ferroelectric capacitor which connects the first data input/output line to the second node.

In the pending rejection, noting the allegation that the volatile memory cells M1-M4 of Papaliolios correspond to the claimed latch circuit, though not expressly stated, the Examiner appears to read the positive power input SP and the negative power input SN of Papaliolios as the claimed first node and second node, respectively. However, in doing so, it is clear that the alleged first ferroelectric capacitor FE0 does ***not*** connect the alleged second data input/output line (i.e., DL that is connected to FE1) to the positive power input SP. Similarly, the alleged second ferroelectric capacitor FE1 does ***not*** connect the alleged first data input/output line (i.e., DL that is connected to FE0) to the negative power input SN. Instead, as is apparent from Papaliolios, the alleged first ferroelectric capacitor FE0 is only connected to the alleged first data input/output line, and the alleged second ferroelectric capacitor FE1 is only connected to the

alleged second data input/output line. It is important to note that Papaliolios expressly discloses such a circuit configuration opposite to that of the present invention, because "[T]his arrangement enables the volatile memory cells M1-M4 to measure the non-volatile configuration state of the ferroelectric capacitor (see, col. 4, lines 59-66)."

In direct contrast and in accordance with one exemplary embodiment of the present invention, the first ferroelectric capacitor 8a connects the second data input/output line 3 to the first node 6, while the second ferroelectric capacitor 8b connects the first data input/output line 2 to the second node 7 (see, e.g., Fig. 1). As a result, the present invention advantageously provides a non-volatile memory cell which enables stable flip-flop operation.

Furthermore, in the event it is asserted that the driving terminal DL connected to ferroelectric capacitor FE1 corresponds to the claimed first data input/output line, and the driving terminal DL connected to ferroelectric capacitor FE0 corresponds to the claimed second data input/output line, such an interpretation of Papaliolios still fails to arrive at the claimed invention, because the alleged first switching element P0 and the alleged second switching element P1 would no longer be connected to the alleged first data input/output line and the alleged second data input/output line, respectively.

Accordingly, as anticipation under 35 U.S.C. § 102 requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference, *Kalman v. Kimberly-Clark Corp., 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983)*, and at a minimum, Papaliolios fails to disclose or suggest the foregoing claim elements, it is clear that Papaliolios does not anticipate claim 1.

III. Conclusion

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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